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# A Review on Machine Learning Enabled Next Generation Electronic Design Automation (EDA)

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**ABSTRACT**: Artificial intelligence (AI) and machine learning (ML) have become the future of design and manufacturing. Machine learning has opened up plenty of new possibilities for computer-aided design (CAD), very large-scale integration (VLSI) design, and their convergence. Recent developments in machine learning offer an opportunity to transform chip design workflow. This paper provides a review of some recent important studies employing machine learning to tackle electronic design automation (EDA) problems.

**KEYWORDS:** Artificial Intelligence, CAD, Electronic Design Automation (EDA), Machine Learning, VLSI.

## I. INTRODUCTION

Electronic Design Automation (EDA) is defined as, "It is a software tool that helps to design an electronic circuits". EDA tool is also known as electronic computer-aided design (ECAD) tool. EDA is one of the most significant fields in electronics engineering. Before the development of EDA tools, the circuit designers were used to rely upon the manually drawn circuit on a paper or some geometric software in order to design a circuit. EDA tool helps to (a) minimize the IC design time, (b) optimize the IC design, (c) reduce the cost of manufacturing and (d) eliminate the manufacturing faults. For designing a variety of electronic chips, the EDA tool offers many benefits, but the EDA tools are very expensive and most of them are difficult to install on a computer.

The rapid and enormously publicized development of data analytics and machine learning (ML) approaches across a wide range of application domains and industries seems to have mostly ignored the semiconductor IC sector [1]. Although the machine learning domain has been in existence for a long time; the recent explosion of open source ML packages & tools, open source data repositories & ML platforms, data manipulation techniques, and the accessibility of open source ML applications have provided the EDA tool developers a set of effective approaches to construct the next generation tools for handling the challenges of next generation chip designs [2].

In the world of big data, machine learning has become a prominent area of study in fields ranging from pattern recognition to classification and finally to prediction. Because of the lack of a large labelled data set, applying machine learning to EDA or very large-scale integration (VLSI) design is more difficult than applying it to basic image or object identification. In fact, the lack of this data makes the first-generation convolutional neural networks (CNN) unsuitable for use, prompting researchers to look into other types of artificial neural networks (ANN) [3].

Over years, EDA software has enhanced semiconductor design production. The integration of machine learning techniques to the toolkit of computational software capabilities used by EDA developers will provide the significant step in production. Recent machine learning research and development (R&D) for EDA has revealed obvious patterns in how it affects EDA tools, processes and design constraints [7].

## II. NEED OF MACHINE LEARNING FOR EDA

Machine learning is playing an increasingly significant part in our lives, and it has been widely applied in a variety of applications. Traditional and deep learning techniques, as well as machine learning methods, succeed at handling classification, detection, and data exploration challenges. With a lack of knowledge, traditional approaches normally fix every problem from the start. Instead of complex analysis, ML algorithms concentrate on collecting high-level features

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or patterns that can be utilized in other similar/related circumstances. As a result, using machine learning approaches to solve EDA challenges is a desirable path to follow.
Owing to the overwhelming complexity of the semiconductor industry, traditional rule-based technology has reached its limits when it comes to solving EDA problems with high dimensionality, discontinuities and nonlinearities. Instead, machine learning is becoming increasingly popular and it is rapidly being used in EDA applications [4].

In the semiconductor industry, machine learning has started to create a new revolution by allowing modeling and simulation to yield unprecedented results. As a consequence, engineers can expect more accurate and efficient design tools and a shift towards wider automation. ML is beginning to have an impact on the EDA tools sector by enabling the tools to recommend solutions to common problems, which will minimizes the design time.

The demand for more functionality, performance and bandwidth in designs is driving design teams to incorporate as many capabilities as possible into their IC designs. Manual analysis of the results generated by EDA tools for resolving violations is a tedious and time-consuming process. Thus, by automating these manual procedures by incorporating ML algorithms can speed up the tape-out process and significantly it optimizes the resources.

## III. LITERATURE REVIEW

In recent years, machine learning for EDA has been a major topic with several papers proposing utilization of ML to enhance EDA approaches.

The paper [1] illustrates how advanced data analytics and machine learning methodologies should be employed for the optimization of physical design, fabrication process as well as IC product yield.

The typical machine learning flow for a verification tool presented in paper [2], firstly it trains the model using the training dataset. Then during the evaluation process, the verification tool uses the trained model once it has been generated for making predictions [Fig. 1].

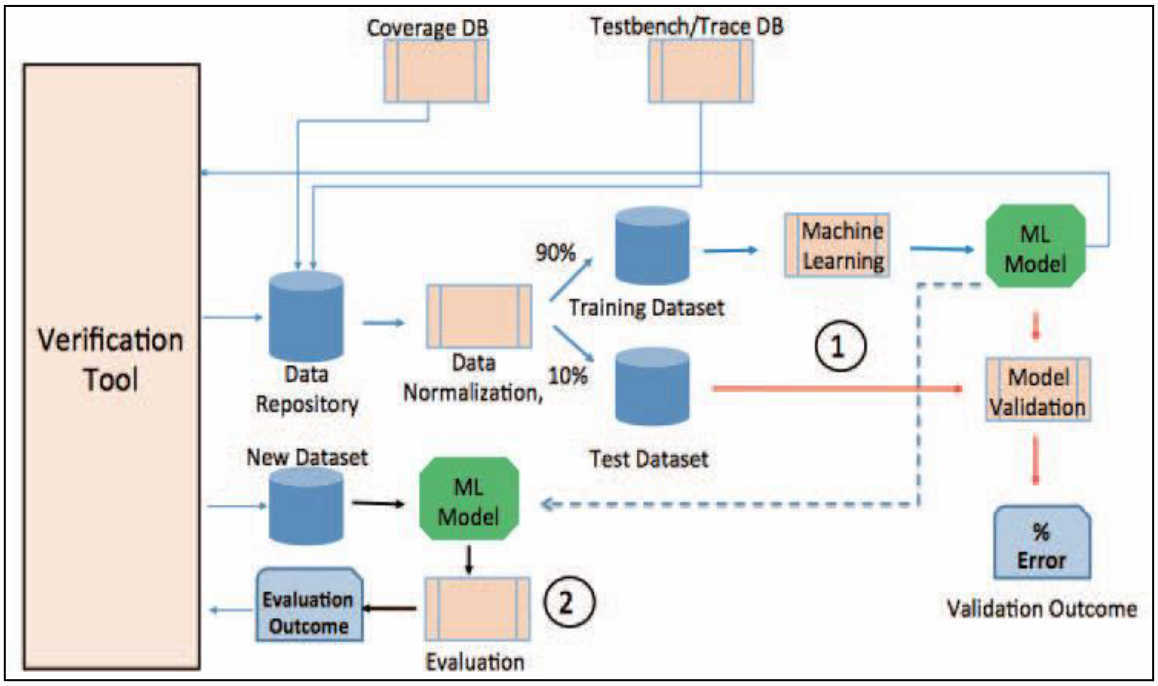


**Fig 1:** Typical Machine Learning Flow for a Verification Tool [2]

The Fig. 2 shows the AI driven VLSI physical design implementation [5] to smartly examine the design space of physical floorplans, timing & tool constraints, and placements. This flow may take use of fast GPU-accelerated placers

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and DL-based deep QoR predictors to enable thousands of rapid iterations within the AI-driven loop while avoiding costly iterations with black-box tools downstream. The AI-driven flow can identify high-quality floorplans, timing constraints and the standard cell placements that can deliver better downstream QoR automatically and rapidly by running within a DRL optimization loop, and then forward those candidate placements to the downstream CTS and routing stages.

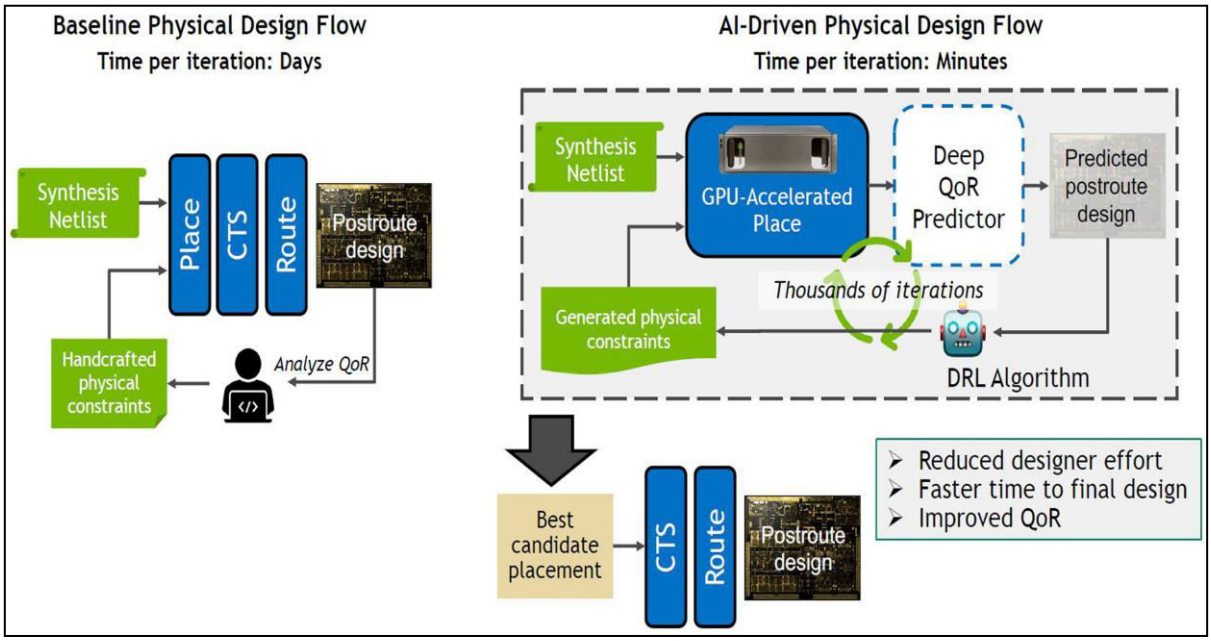


**Fig. 2:** VLSI Physical Design Implementation Flows [5]

ML models can forecast dynamic power by predicting the propagation of switching activity factors via a logic netlist without simulation, resulting in faster and more accurate power estimations. The IR drop analysis problem is solved by PowerNet10, which predicts IR drop directly from per-cell power distributions. With the aid of AI, ParaGraph which is a GNN that predicts analog layout parasitics and device characteristics directly from circuit diagrams [5].

Furthermore, machine learning algorithms have the potential to provide high-quality solutions for numerous NP-complete (NPC) problems that are common in the EDA industry, whereas traditional methods take a considerable amount of time and resources. The study [6] discusses some of the difficulties and opportunities for next-generation physical design by utilizing machine learning. P&R tools aim to solve an ensemble of NPC problems in (pseudo) linear time.

The architecture of most existing EDA techniques is restricted by CPU parallelism, and their performance peaks at 8-16 cores. New EDA methods must leverage the potential of heterogeneous parallelism, which consists of many core CPUs and GPUs to achieve new revolutionary outcomes. However without a proper software framework to help developers in the implementation complexities inherent into heterogeneous parallelism, these milestones will be too difficult to attain. By utilizing the capabilities of machine learning systems, this study [8] provides GPU acceleration for placement and timing analyses, where 500-fold speedup for static timing analysis on a million-gate design was obtained.

Every design will create pre-route and post-route data but more significantly, the data will illustrate how the design evolved over time by demonstrating what the engineer did to meet timing goals. These data may be used to train the ML model, so that when it meets that design or one very similar to it, it will be able to anticipate where to place blocks initially with better accuracy and in a shorter period of time. Better results will be delivered faster at the post-route stage if the pre-route results are more accurate [9]. The Fig. 3 shows the time prediction in placement and routing using machine learning technique.

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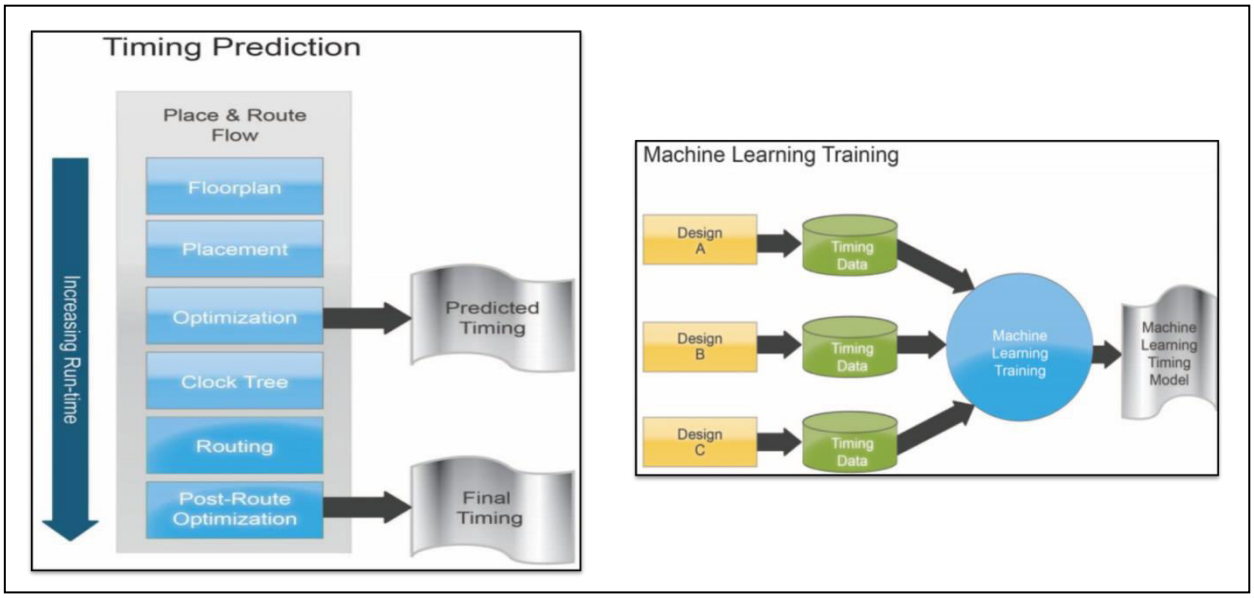


**Fig. 3:** Time Prediction in Placement and Routing Using ML [9]

## IV. BENEFITS

Following are some of the benefits of adapting machine learning for EDA:

a) At each stage of the chip development process, ML generated models gives improved feedback to engineers by showing the intended performance.

b) The chip development process is more efficient when the engineer has trained models to assist him to analyze the design and identify when a rule has been violated.

c) Machine learning can assist engineers in identifying and interpreting errors with their designs more quickly, allowing them to be more productive.

d) Another advantage of ML for EDA is increased efficiency, which translates to faster turnaround times, better analytical flexibility and more simulation coverage.

## V. CONCLUSION

For optimal performance, several machine learning approaches were used in the development of next-generation EDA tools. From this brief survey of machine learning for EDA, it is clear that AI will have a major impact on how the VLSI design is done today. Many human design activities will be automated, enabling designers to focus on the most challenging and complex design issues.

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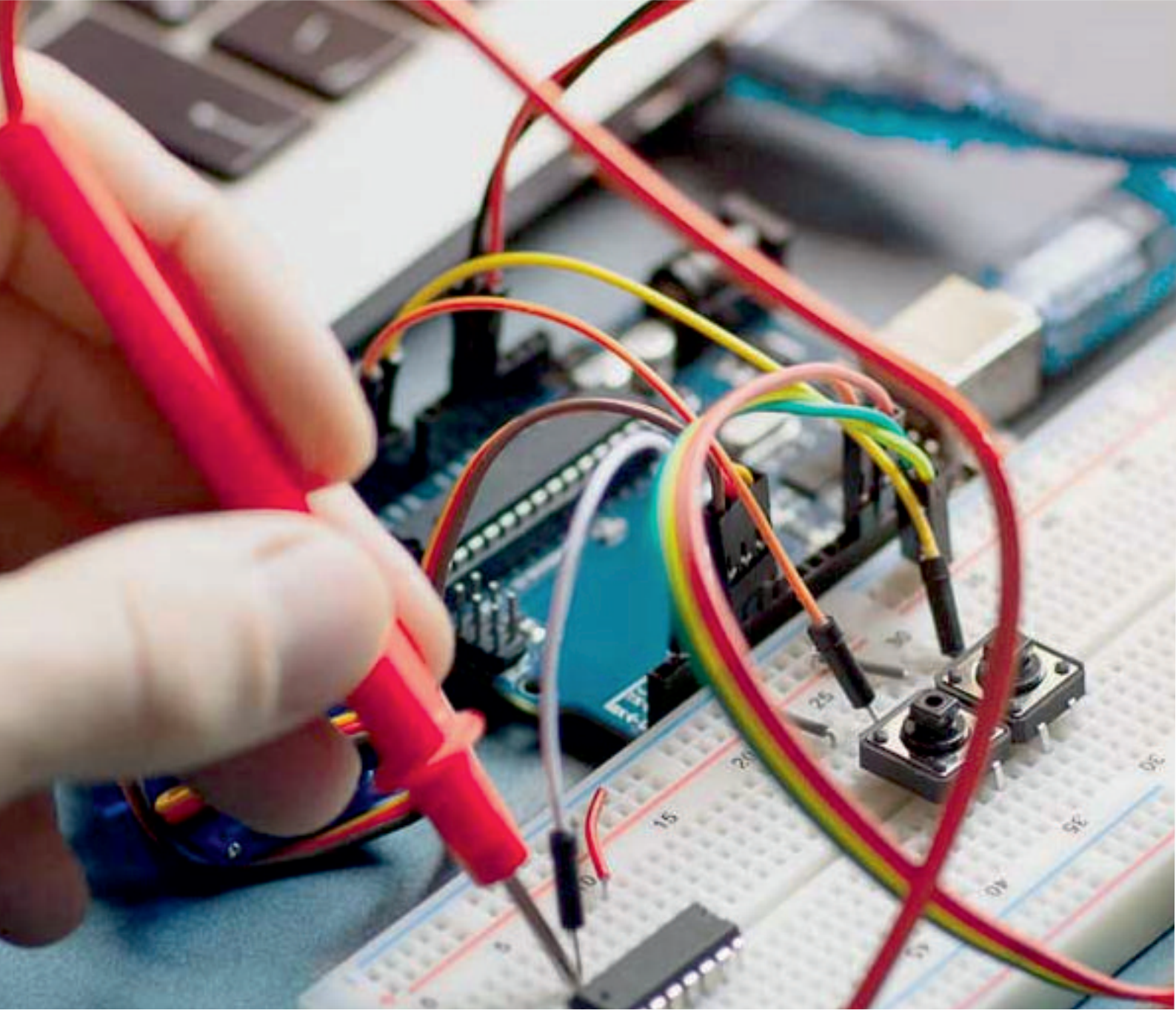

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